

REMARKS

Applicants respectfully request the entry of these amendments prior to substantive examination.

Respectfully submitted,

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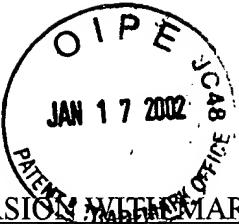
I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to the Commissioner for Patents, Washington, D.C. 20231, on the below date.

Date: George S. Farber 11/2/01

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VERSION WITH MARKINGS TO SHOW CHANGES MADE NOVEMBER 1, 2001

In the Abstract:

An external defibrillator/pacer (8) includes an output circuit (14) with four legs arrayed to form an H-bridge coupled to an energy storage capacitor. The energy storage capacitor delivers an external defibrillation pulse with stored energy during a defibrillation mode and an external pacing pulse during a pacing mode. Each leg of the output circuit contains a switch (SW1-SW4). In a defibrillation mode, pairs of switches in the H-bridge are selectively switched to generate a biphasic defibrillation pulse. Three switches (SW1, SW3, SW4) are silicon controlled rectifiers (SCRs). Gate drive circuits (51, 53, 54) are coupled to the SCRs to bias the SCRs with a voltage that allows the SCRs in response to control signals. One switch (SW2) includes an insulated gate bipolar transistor (IGBT). A gate drive circuit (52) is coupled to the gate of the IGBTs to provide a slow turn-on and a fast turn-off of the IGBT. In a pacing mode, a bypass circuit or current source circuit is used to provide a current path bypassing an SCR switch (SW3), which cannot be triggered by the relatively low current of pacing pulses. One of the SCRs (SW4) may be replaced with an IGBT to allow generation of the pacing pulse with opposite polarity of the first phase of the defibrillation pulse.

In the Claims:

New Claims 35-67 have been added.

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